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CofC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble Jr. et al.

Examiner: Trinh, Michael

Patent No.: 6,764,901 *B2*

Group Art Unit: 2822

Issue Date: July 20, 2004

Docket No: 303.379US2

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

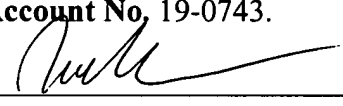
**Certificate
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of Correction**

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- ☒ Request for Certificate of Correction.
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer No: 21186

By: 
Name: Viet V. Tong
Reg. No. 45,416
VVT:CMG:mm1

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria VA 22313-1450, on this 10 day of December 2004.

Michael M Linse
Name


Signature

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Patent 6,764,901

PATENT

IN UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 6,764,901 B2

Docket No: 303.379US2

Issue Date: July 20, 2004

Patentee: Wendell P. Noble Jr. et al.

Customer No.: 21186

Confirmation No.: 1158

Title CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR



REQUEST FOR CERTIFICATION OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States patent. Two copies of the text of the Certificate in the suggested form are enclosed.

Pursuant to 1.20(a), enclosed please find a check in the amount of \$100.00.

Issuance of the Certificate of Correction would neither expand nor contract the scope of the claims as properly allowed, and re-examination is not required.

The Examiner is authorized to charge any additional fees or credit overpayment to Deposit Account No.19-0743

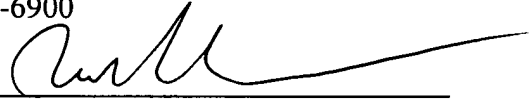
Respectfully Submitted

WENDELL P. NOBLE JR. ET AL.

By their Representatives,


SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6900

Date : 6 December 2004

By: 
Viet V. Tong
Reg. No: 45,416
VVT:CMG: mml

CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 6 day of December 2004

Michael M Linse
Name


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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

page 1 of 3

PATENT NO : 6,764,901 *B2*

DATED : July 20, 2004

INVENTOR(S) : Noble et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the face page, in field (56), under "Other Publications", in column 2, line 7, after "Parameters" delete "for".

On page 3, in field (56), under "Other Publications", in column 1, line 26, delete "et al." and insert - - et al. - -, therefor.

On page 3, in field (56), under "Other Publications", in column 1, line 56, after "section" insert - - : - -.

On page 3, in field (56), under "Other Publications", in column 2, line 31, delete "14" and insert - - 34 - -, therefor.

On page 3, in field (56), under "Other Publications", in column 2, line 37, delete "Honolulu" and insert - - Honolulu - -, therefor.

On page 3, in field (56), under "Other Publications", in column 2, line 37, insert - - (- - before "Jun."

On page 3, in field (56), under "Other Publications", in column 2, line 38, delete "Photoluminescence" and insert - - Photoluminescence - -, therefor.

On page 4, in field (56), under "Other Publications", in column 1, line 5, delete "Metallizatin" and insert - - Metallization - -, therefor.

On page 4, in field (56), under "Other Publications", in column 1, line 12, delete "462" and insert - - 461 - -, therefor.

On page 4, in field (56), under "Other Publications", in column 1, line 42, delete "A1303" and insert - - A1303 - -, therefor.

MAILING ADDRESS OF SENDER:

SCHWEGMAN, LUNDBERG, WOESSNER, & KLUTH, P.A.
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Minneapolis, MN 55402

Atty Docket No: 303.379US2

PATENT NO. 6,764,901

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On page 4, in field (56), under "Other Publications", in column 2, line 18, delete "Honoluly" and insert - - Honolulu - -, therefor.

On page 4, in field (56), under "Other Publications", in column 2, line 24, delete "Parasite" and insert - - Parasitics - -, therefor.

On page 5, in field (56), under "Other Publications", in column 1, line 32, delete "1991" and insert - - 1993 - -, therefor.

On page 5, in field (56), under "Other Publications", in column 1, line 39, delete "Verdonct" and insert - - Verdonckt - -, therefor.

On page 5, in field (56), under "Other Publications", in column 1, line 48, delete "Characterization" and insert - - Characteristics - -, therefor.

On page 5, in field (56), under "Other Publications", in column 2, line 48, delete "Signal- Integrated" and insert - - Signal Integrated - -, therefor.

In column 1, line 37, delete "an" and insert - - a - -, therefor.

In column 2, line 50, after "trench" insert - - . - -.

In column 6, line 32, after "depicted here." delete "Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 201 of, for example, p- silicon. First source/drain region 206 and second source/drain region 210 each comprise, for example, n+ silicon and body region 208 comprises P-silicon" and insert - - Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 201 of, for example, p- silicon. First source/drain region 206 and second source/drain region 210 each comprise, for example, n+ silicon and body region 208 comprises P- silicon. - - as a new paragraph on line 33.

In column 7, line 1, delete "late" and insert - - plate - -, therefor.

In column 8, line 49, delete "322" and insert - - 332 - -, therefor.

In column 9, line 3, delete "322" and insert - - 332 - -, therefor.

In column 11, line 58, in Claim 17, delete "claim 13" and insert - - claim 16 - -, therefor.

In column 11, line 61, in Claim 18, delete "claim 13" and insert - - claim 16 - -, therefor.

In column 16, lines 52 - 53, in Claim 39, after "the top" delete "even with the top".

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In column 17, line 28, in Claim 40, after "substrate," delete "a".

In column 18, line 3, in Claim 40, after "top" delete "even with the top".

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